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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,553	NODA ET AL.	
	Examiner	Art Unit	
	AIMEE J. LI	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1-12 and 14*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 July 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/24/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 and 14 have been considered. Claim 13 has been canceled as per Applicants' request. Claims 1, 6, and 8 have been amended as per Applicants' request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 09 October 2009, One month Extension of Time, and IDS as filed 24 November 2009.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 24 November 2009 was filed after the mailing date of the Office Action on 16 June 2009. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

4. Examiner notes that the Patent Application Publication cited had been considered in a previously submitted IDS. As such, the Patent Application Publication cannot be considered a second time.

Response to Arguments

5. Applicant's arguments filed 09 October 2009 have been fully considered but they are not persuasive.

6. Applicants' argue in essence on page 8 "…In the presently claimed invention, the first processor (GPU) performs both a main routine and a subroutine called by the main routine. The second processor only helps the call and return process executed inside the first processor, and does not perform the main routine or the subroutine…". This has not been found persuasive.

The claim language in question states, taking claim 1 as exemplary, "...returning to the main routine upon completion of processing of a subroutine called by the call instruction and performed by the first processor...". The "performed by the first processor" phrase modifies the "main routine". Consequently, the claims do not explicitly state, as suggested by the arguments, that the subroutine called by the main routine is performed by the first processor (GPU) and that the second processor only helps the call and return process, not executing the main routine and call subroutine. Goettsu does teach that the main routine is executed in the first processor, as cited in the rejection above, which is all that is required by the claim language. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the second processor only helps the call and return process) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

7. Applicants' argue in essence on pages 8-10 "...it is respectfully submitted that there is no description about the destination address in Goettsu. This is because the Power PC itself executes the call instruction, therefore there is no need to divide the destination address." This has not been found persuasive. The claim language in question, taking claim 4 as exemplary, states "...extract a call destination address or a jump destination address stored dividedly in formats of the call instruction or the jump instruction...". This claim language merely requires that the call destination address is stored in the call instruction format, which is separate, i.e. divided, from the call address destination stored in the call instruction format. Consequently, the claims do not explicitly require, as suggested by the arguments, the destination address is stored

"in two instruction codes regardless of which instruction the processors execute (arguments page 9)". In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the destination address is stored in two instruction codes regardless of which instruction the processors execute) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-5, 8-12, and 14 are rejected under 35 U.S.C. 102(b) as being taught by Goettsu et al., Japanese Patent H09-231093 (herein referred to as Goettsu). Examiner notes that the following citations are from the machine translation provided.

10. Referring to claim 1, Goettsu has taught a multiprocessor system comprising

a. a first processor and a second processor (Goettsu Drawing 12, elements 61 and 62), wherein:

b. the first processor comprises an interrupt generation unit which generates an interrupt to the second processor when the first processor executes a predetermined call instruction in a running main routine (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2), the

interrupt being for requesting to store a return address for returning to the main routine upon completion of processing of a subroutine called by the call instruction and performed by the first processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2); and

c. the second processor comprises an address save unit which saves a the return address the return address to a predetermined memory area when the second processor receives an interrupt from the interrupt generation unit (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2 – In regards to Goettsu, when a call PowerPC program occurs, the x86 is sent the instruction to perform the call operations, such as saving the return address, since the PowerPC does not have the capability.).

11. Referring to claim 2, Goettsu has taught the multiprocessor system according to claim 1, wherein:

a. the interrupt generation unit generates an interrupt to the second processor again when a predetermined return instruction is executed in the subroutine (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2); and

b. the second processor further comprises an address notification unit which communicates the return address to the first processor when receiving the re-generated interrupt (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

12. Referring to claim 3, Goettsu has taught the multiprocessor system according to claim 1, wherein the first processor comprises a fetcher which fetches an instruction (Goettsu Drawing 1, element 6); and the return address is set as a target address to be accessed by the fetcher (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

13. Referring to claim 4, Goettsu has taught a multiprocessor system comprising a first processor and a second processor (Goettsu Drawing 12, elements 61 and 62), wherein:

a. the first processor comprises an interrupt generation unit which generates an interrupt to the second processor when the first processor executes a predetermined call instruction or jump instruction (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2), the interrupt being for requesting to extract a call destination address or a jump destination address stored dividedly in formats of the call instruction or the jump instruction and an accompanying execution stop instruction (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2 – In regards to Goettsu, when the PowerPC executes a call instruction, the destination address and return address are 64 bits and are stored in two parts by the x86 system, since the x86 is only 32 bits.); and

b. the second processor comprises:

   i. an address extraction unit which extracts a the call destination address or the jump destination address when the second processor receives the interrupt from the first processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2); and

ii. an address notification unit which communicates the acquired call destination address or jump destination address to the first processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

14. Referring to claim 5, Goettsu has taught the multiprocessor system according to claim 4, wherein:

a. the first processor further comprises a fetcher which fetches an instruction (Goettsu Drawing 1, element 6); and

b. the call destination address or the jump destination address is set as a target address to be accessed by the fetcher (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

15. Referring to claim 8, Goettsu has taught a method of executing a program in a multiprocessor system, the method comprising, executing a call instruction in a main routine running by a first processor, generating an interrupt for delegating to a second processor the task of saving a return address for returning to the main routine upon completion of processing of a subroutine called by the call instruction and performed by the first processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

16. Referring to claim 9, Goettsu has taught the method of executing a program in a multiprocessor system according to claim 8, wherein:

a. if a stack area inside the first processor has a free space, the first processor saves the return address to the stack area by itself (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2); and

b. if the stack area has no free space, the save of the return address is delegated to the second processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

17. Referring to claim 10, Goettsu has taught the method of executing a program in a multiprocessor system according to claim 8, wherein:

a. if the call instruction does not explicitly instruct to delegate the task of saving the return address to the second processor, the first processor saves the return address to a stack area built in itself (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2); and

b. if the call instruction explicitly instructs to delegate the task of saving the return address to the second processor, the first processor delegates the task of saving the return address to the second processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

18. Referring to claim 11, Goettsu has taught a method of executing a program in a multiprocessor system, the method comprising, executing a call instruction or a jump instruction by a first processor, generating an interrupt for delegating a task of acquiring a full address of a call destination address or a jump destination address stored dividedly in formats of the call instruction or the jump instruction and an accompanying execution stop instruction to a second processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

19. Referring to claim 12, Goettsu has taught a method of executing a program in a multiprocessor system according to claim 11, wherein delegating a task of acquiring the full

address of the call destination address or the jump destination address to a second processor, if the number of bits of the call destination address or the jump destination address exceeds the number of bits acquirable by the first processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

20. Referring to claim 14, Goettsu has taught a method of executing a program in a multiprocessor system according to claim 11, wherein delegating the task of acquiring the full address of the call destination address or the jump destination address to a second processor if the call instruction or the jump instruction explicitly instructs to delegate the task of acquiring the call destination address or the jump destination address to the second processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goettsu et al., Japanese Patent H09-231093 (herein referred to as Goettsu) in view of Dye, U.S. Patent Number 5,706,478 (herein referred to as Dye).

23. Referring to claim 6, Goettsu has taught a multiprocessor system comprising a co-processor and a main processor (Goettsu Drawing 12, elements 61 and 62), wherein

a. the co-processor processor comprises:

iii. a decoder which decodes the read instructions sequentially (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2); and

iv. an interrupt generation unit which generates a shift interrupt to the main processor when a decoded instruction is a predetermined call instruction included in a main routine (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2) and generates a return interrupt to the main processor when a decoded instruction is a return instruction included in a subroutine called by the call instruction and performed by the graphics processor (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2), the shift interrupt being for requesting to store a return address for returning to the main routine upon completion of processing of the subroutine, and the return interrupt being for requesting to transfer the return address (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2),

b. the main processor comprises:

v. an address save unit which saves the return address to a predetermined memory when the main processor receives the shift interrupt from the interrupt generation unit (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2); and

vi. an address notification unit which reads the return address from the predetermined memory and communicates the return address to the graphics processor when the main processor receives the return interrupt from the interrupt generation unit (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2), and

c. the return address communicated to the graphics processor is set as a target address (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2).

24. Goettsu has not taught

a. a graphics co-processor (Dye Figure 1, element 100) comprising a direct memory access controller (DMAC) which reads instructions written in a display list from a memory sequentially (Dye column 13, line 47 to column 14, line 5); and

b. instruction addresses to be accessed by the DMAC (Dye column 13, line 47 to column 14, line 5).

25. A person of ordinary skill in the art at the time the invention was made would have recognized that incorporating the graphics co-processor of Dye increases processing speed for graphics (Dye column 3, lines 22-27). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the graphics co-processor of Dye in the device of Goettsu to increase graphics processing speed.

26. Referring to claim 7, Goettsu in view of Dye has taught a multiprocessor system comprising a graphics processor (Dye Figure 1, element 100) and a main processor (Goettsu Drawing 12, elements 62), wherein

a. the graphics processor comprises:

vii. a direct memory access controller (DMAC) which reads instructions written in a display list from a memory sequentially (Dye column 13, line 47 to column 14, line 5);

viii. a decoder which decodes the read instructions sequentially (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2); and

ix. an interrupt generation unit which generates an interrupt to the main processor when a decoded instruction is a predetermined call instruction or a jump instruction (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2) included in the display list, the interrupt being for requesting to extract a call destination address or a jump destination address stored dividedly in formats of the call instruction or the jump instruction and an accompanying execution stop instruction (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2),

b. the main processor comprises an address notification unit which acquires a the call destination address or a the jump destination address (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2), and communicates the call destination address or the jump destination address to the graphics processor when the main processor receives the interrupt from the

interrupt generation unit (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2), and

c. the call destination address or the jump destination address communicated to the graphics processor is set as a target address (Goettsu paragraphs 0007-0008, 0010, 0017-0019, and 0021-0022, Drawing 1, and Drawing 2) to be accessed by the DMAC (Dye column 13, line 47 to column 14, line 5).

Conclusion

27. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

28. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to AIMEE J. LI whose telephone number is (571)272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aimee J Li/
Primary Examiner, Art Unit 2183

31 January 2010